IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An Arithmetic and Logic Unit (ALU), comprising:

at least first and second sub-ALUs,

each sub-ALU configured to operate on at least two multi-bit numbers to generate a multi-bit output result,

each of the first and second sub-ALUs including a plurality of slices, each configured to perform at least one operation on a set of bits including at least one bit from each of the at least two multi-bit numbers operated on by the sub-ALU in which it is included and generate at least one bit of the multi-bit output result of the sub-ALU in which it is included, and

wherein the slices of the first and second sub-ALUs are interleaved such that pairs of adjacent slices in the ALU include one slice from the first sub-ALU and one slice from the second sub-ALU.

2. (Original) The ALU of claim 1 wherein the slices of the first and second sub-ALUs are bitslices.

3. (Original) The ALU of claim 2 wherein each of the bitslices of the first sub-ALU includes a gate configured to perform a logical operation.

4. (Original) The ALU of claim 3 wherein the gate is configured to receive two input bits and generate one output bit.

5. (Original) The ALU of claim 3 wherein the logical operation is logical AND operation.

6. (Original) The ALU of claim 2 wherein the bitslices of the first sub-ALU are connected in series.

7. (Original) The ALU of claim 6 wherein the bitslices of the second sub-ALU are connected in series.

8. (Original) The ALU of claim 6 wherein each of the bitslices of the first sub-ALU includes an adder configured to add at least two bits to generate a carry bit to a next consecutive bitslice of the first sub-ALU.

9. (Original) The ALU of claim 2, wherein each pair of adjacent bitslices of the ALU comprises a first bitslice of the first sub-ALU and a second bitslice of the second sub-ALU; and wherein:

the first bitslice has a first input and a first output, a second bitslice has a second input and a second output; and

the first output is connected to the second input, and the second output is connected to the first input.

10. (Original) The ALU of claim 1 wherein the slices of the first and second sub-ALUs are function slices.

11. (Original) The ALU of claim 10 wherein the function slices of the first sub-ALU are connected in series and the function slices of the second sub-ALU are connected in series.

12. (Currently Amended) A method for implementing at least first and second sub-ALUs to form an ALU, each of the first and second sub-ALUs including a plurality of slices, the method comprising:

interleaving the slices of the first and second sub-ALUs such that pairs of adjacent slices in the ALU include one slice from the first sub-ALU and one slice from the second sub-ALU, wherein each sub-ALU is configured to operate on at least two

multi-bit numbers to generate a multi-bit output result, and wherein each slice is configured to perform at least one operation on a set of bits including at least one bit from each of the at least two multi-bit numbers operated on by the sub-ALU in which it is included and generate at least one bit of the multi-bit output result of the sub-ALU in which it is included.

13. (Original) The method of claim 12 wherein the slices of the first and second sub-ALUs are bitslices.

14. (Original) The method of claim 13 further comprising connecting the bitslices of the first sub-ALU in series.

15. (Original) The method of claim 14 further comprising connecting the bitslices of the second sub-ALU in series.

16. (Original) The method of claim 13, wherein each pair of adjacent bitslices of the ALU comprises a first bitslice of the first sub-ALU and a second bitslice of the second sub-ALU, and further comprising:

providing a first input and a first output for the first bitslice;
providing a second input and a second output for the second bitslice;
connecting the first output to the second input; and
connecting the second output to the first input.

17. (Original) The method of claim 12 wherein the slices of the first and second sub-ALUs are function slices.

18. (Original) The method of claim 17 further comprising connecting the function slices of the first sub-ALU in series and connecting the function slices of the second sub-ALU in series.

19. (Currently Amended) A method for implementing at least first and second ALUs, each ALU configured to operate on at least two multi-bit numbers to generate a multi-bit output result, the first ALU having a first input side and a first output side, the second ALU having a second input side and a second output side, the method comprising:

arranging the first and second ALUs using one of first and second arrangements, wherein the first arrangement comprises arranging the first output side closer to the second output side than to the second input side, the second arrangement comprises arranging the first input side closer to the second input side than to the second output side.

20. (Original) The method of claim 19 wherein arranging the first and second ALUs comprises using the first arrangement.

21. (Original) The method of claim 19 further comprising:
connecting a first output of the first ALU to a first input of the second ALU; and
connecting a second output of the second ALU to a second input of the first ALU.

22. (Original) The method of claim 19 wherein each of the first and second ALUs has at least first and second sub-ALUs, each of the first and second sub-ALUs including a plurality of slices wherein the slices of the first and second sub-ALUs are interleaved.

23. (Currently Amended) A digital circuit, comprising at least first and second ALUs, each ALU configured to operate on at least two multi-bit numbers to generate a multi-bit output result, the first ALU having a first input side and a first output side, the second ALU having a second input side and a second output side, wherein the first and second ALUs are arranged in one of first and second arrangements, wherein

in the first arrangement, the first output side is closer to the second output side than to the second input side, and

in the second arrangement, the first input side is closer to the second input side than to the second output side.

24. (Original) The digital circuit of claim 23 wherein a first output of the first ALU is connected to a first input of the second ALU and a second output of the second ALU is connected to a second input of the first ALU.

25. (Original) The digital circuit of claim 23 wherein each of the first and second ALUs has at least first and second sub-ALUs, each of the first and second sub-ALUs including a plurality of slices wherein the slices of the first and second sub-ALUs are interleaved.

26. (Original) The digital circuit of claim 23 wherein the slices of the first and second sub-ALUs comprises one of bitslices and function slices.